

Application No.: 10/065,524

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Docket No.: JCLA8269

**REMARKS****Present Status of the Application**

This Office Action rejected all presently-pending claims 1-11. Specifically, the Office Action rejected claims 2, 3, 6, 7, 10 and 11 under 35 U. S. C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 5 are rejected under 35 U.S.C. 102(b), as being anticipated by US Patent Number 5,628,001 to Cepuran ("Cepuran"). The Office Action also rejected claims 2, 3, 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over Cepuran, and further in view of US Patent Number 6,163,826 to Gulick et al ("Gulick"). The Office Action also rejected claims 2, 3, 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over Cepuran, and further in view of US Patent Application Publication Number 2002/0023190 to Peng ("Peng"). The Office Action also rejected claims 4 and 8 under 35 U.S.C. 103(a) as being unpatentable over Cepuran, and further in view of US Patent Number 6,057,729 to Nomura ("Nomura"). The Office Action rejected claim 9 under 35 U.S.C. 103(a), as being unpatentable over Cepuran and Nomura. The Office Action rejected claims 10 and 11 under 35 U.S.C. 103(a), as being unpatentable over Cepuran and Nomura, and further in view of Gulick. The Office Action rejected claims 10 and 11 under 35 U.S.C. 103(a), as being unpatentable over Cepuran and Nomura, and further in view of Peng. Reconsideration of these pending claims is respectfully requested.

**BEST AVAILABLE COPY**

Application No.: 10/065,524

Docket No.: JCLA8269

**Discussion of Claim Rejections-35 U.S.C. 112, second paragraph**

The interpretation by the Examiner on the definition of north-bridge and south-bridge is acceptable by the applicants. However, the definition of north-bridge and south-bridge is not limited to the interpretation by the Examiner. Applicants wish to clarify that the foregoing description has been made in response to the rejections made under 35 U.S.C. § 112, second paragraph, and not in response to the rejections made based on prior art. Indeed, Applicants submit that no substantive limitations have been added to the claims. Therefore, no prosecution history estoppels arises. This description is promptly filed to place the above-captioned case in condition for allowance. Applicants believe that this description places the claims in condition for allowance. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

**Response to Examiner's Reply and Discussion of Office Action Rejections-35 U.S.C. 102(b)**

The Office Action rejected claims 1 and 5 are rejected under 35 U.S.C. 102(b), as being anticipated by US Patent Number 5,628,001 to Cepuran. However, the applicants respectfully disagree the rejection for at least the reasons below.

To anticipate a claim, the reference must cite all limitations. Cepuran discloses a communication system capable of power conservation. As shown in FIG. 2, the first and second circuit elements 106 and 112 are operative to transmit information upon the bus 136 to each other. Clock signal generator 148 generates a clock signal (154 and 160) to the circuit elements 106 and 112. Clock signal generator 148 generates a low-frequency signal and a high-frequency signal. A control signal 166, generated by the first circuit element 106 is applied to the clock signal

**BEST AVAILABLE COPY**

Application No.: 10/065,524

Docket No.: JCLA8269

generator 148 to control selection of the frequency of the clock signal generated thereat. When neither the first circuit element 106 nor the second circuit element 112 transmits a signal upon the bus 136, the clock signal generator 148 generates the low-frequency clock signal. However, when the first circuit element 106 or the second circuit element 112 is operative to transmit information upon the bus 136, the first circuit element 106 provides the control signal 166 to the clock signal generator 148 and responsive to the control signal 166, the clock signal generator 148 generates the high-frequency clock signal. Therefore, the rate of information transmission between circuit elements 106 and 112 is increased.

In regard to Claim 1, the first and second control chips receive a transfer rate switching command. But in Cepuran, the circuit elements 106 and 112 receive the clock signals 154 and 160 from the generator 148. As known, the clock signal determines the operation rates of the circuit elements 106 and 112 by itself. The clock signal 154/160 increases the operation rates of the circuit elements 106 and 112 only if information is to be transmitted on the bus and reduces the operation rates of the circuit elements 106 and 112 only if the transmission is completed. But in claim 1, the transfer rate switching command does not change the transfer rate of the first and second control chips by itself, if without the additions of the bus release connect command and the bus re-connect command. And as known, the clock signals provided to the first and second control chips are provided by a system clock generator. The transfer rate switching command would not be used as the clock signals and vice versa. It is clear that the clock signals 154/160 in Cepuran are different from the transfer rate switching command in claim 1. Therefore, Cepuran does not disclose a feature of the first and second control chips receiving a transfer rate switching

**BEST AVAILABLE COPY**

Application No.: 10/065,524

Docket No.: JCLA8269

command because a clock signal in Cepuran is totally different from the transfer rate switching command in Claim 1 of the application.

Secondly, in Cepuran, the first circuit element 106 issues a control signal to the clock signal generator for generating a low-frequency clock signal if no information is transmitted or when information transmission is completed, so that the first and second circuit elements operate at low frequency. But in Claim 1 of the application, the first control chip issues a bus release connect command to make the first and second control chips enter into the bus release connect state if there is no data transaction processed or the data transaction process is finished. The bus release connect state implies the first and second control chips temporality "logically" disconnect from the bus. Therefore, Cepuran does not teach this feature.

Thirdly, Cepuran's first circuit element 106 provides a control signal to the clock signal generator for generating a high-frequency clock signal when information is transmitted, so that the first and second circuit elements operate at high frequency. But in Claim 1 of the application, the first control chip or the second control chip issue a bus re-connect command to make the first and second control chips reconnect to the bus. Therefore, Cepuran does not teach this feature because Cepuran's control signal for making the first and second circuit elements operate at high frequency is different from the bus re-connect command in claim 1 of the application.

Furthermore, from FIG. 2 and FIG. 7 of Cepuran, it is clear that the operation rates of the first and second circuit elements have to be higher if information is to be transmitted on the bus and lower if the information transmission is completed or no information is transmitted and the generator 148 always generates clock signals to the elements 106 and 112. But in Claim 1, the

Application No.: 10/065,524

**BEST AVAILABLE COPY** Docket No.: JCLA8269

transfer rate is changed only if a transfer rate switching command is received by the first and second control chips and the transfer rate switching command is not always issued.

Thus, Cepuran does not anticipate claim 1, and the rejection should be withdrawn.

Similarly, in Claim 5, the first and second control chips receive a transfer rate switching signal before data transfer on the bus is interrupted. But in Cepuran, the first and second circuit elements 106 and 112 always receive the clock signals 154/160 from the generator 148.

Thus, Cepuran does not anticipate claim 5, and the rejection should be withdrawn.

**Discussion of Office Action Rejections-35 U.S.C. 103(a)**

The Office Action also rejected claims 2, 3, 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over Cepuran, and further in view of US Patent Number 6,163,826 to Gulick. The Office Action also rejected claims 2, 3, 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over Cepuran, and further in view of Peng. The Office Action also rejected claims 4 and 8 under 35 U.S.C. 103(a) as being unpatentable over Cepuran, and further in view of Nomura. The Office Action rejected claim 9 under 35 U.S.C. 103(a), as being unpatentable over Cepuran and Nomura. The Office Action rejected claims 10 and 11 under 35 U.S.C. 103(a), as being unpatentable over Cepuran and Nomura, and further in view of Gulick. The Office Action rejected claims 10 and 11 under 35 U.S.C. 103(a), as being unpatentable over Cepuran and Nomura, and further in view of Peng. Applicants respectfully traverse the rejections for at least the reasons set forth below.

As discussed above, because Cepuran does not teach/suggest/disclose at least the above features of claims 1 and 5, the combination of Cepuran and Gulick would not render claims 2, 3,

**BEST AVAILABLE COPY**

Application No.: 10/065,524

Docket No.: JCLA8269

6 and 7 obvious. Similarly, the combination of Cepuran and Peng would not render claims 2, 3, 6 and 7 obvious. The rejections should be withdrawn.

More specially, in regarding to claims 4, 8 and 9, as discussed above, Cepuran does not disclose the similar features in claim 1 of the application. Furthermore, in FIG. 6 of Nomura, the shift register 525 is use to shift the IN and output the shifted IN as IN0~IN7 to the register 526 and then the register 526 temporarily stored IN0~IN7 and outputs IN0~IN7 as OUT0 ~ OUT7. It is known that a clock signal is used to trigger the operation of the shift register 525 and the register 526 and the shift register 525 and the register 526 would never temporarily store the clock signal. The combination of Ccpuran and Nomura would not render claims 4, 8 and 9 obvious. The rejections should be withdrawn.

If independent claim 9 is allowable over the prior art of record, then its dependent claims 10 and 11 are allowable as a matter of law, because the dependent claims contain all features/elements of the independent claim 9. Additionally and notwithstanding the foregoing reasons for the allowability of claim 9, the dependent claims 10 and 11 recite further features and/or combinations of features (as is apparent by examination of the claims themselves) that are patentably distinct from the prior art of record.

**Prior Art Made of Record**

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

**BEST AVAILABLE COPY**

Application No.: 10/065,524

Docket No.: JCLA8269

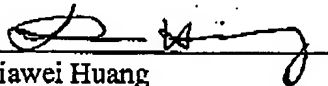
**CONCLUSION**

For at least the foregoing reasons, it is believed that the pending claims 1-11 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date: 10/7/2005

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